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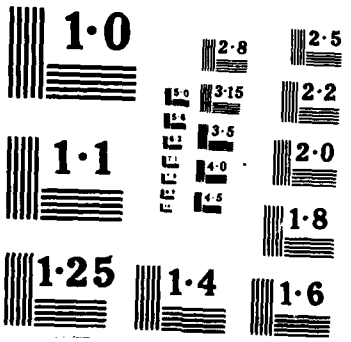
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NOVEL Si-BASED MATERIALS AND DEVICE STRUCTURES BY MOLECULAR BEAM EPITAXY

FINAL REPORT

K. L. WANG

JUNE 1986

U. S. ARMY RESEARCH OFFICE

DAAG 29-83-K-0070

UNIVERSITY OF CALIFORNIA, LOS ANGELES

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The final report describes the technical tasks and accomplishments during the contractual period from April 25, 1983 to April 24, 1986. Research findings in four scientific areas, (a) MBE growth, (b) heterojunction properties, (c) superlattice and quantum well structural devices, and Si on insulator by MBE are summarized. Details of these results are referred to the journal publications attached. In addition to scientific publications, the results of this research also help industrial development of commercial molecular beam epitaxy systems in U.S.

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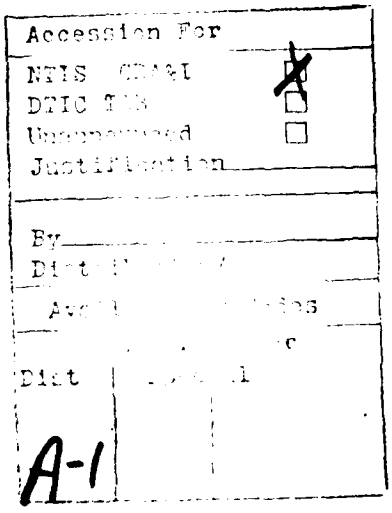


1. ABSTRACT

The final report describes the technical tasks and accomplishments during the contractual period from April 24, 1983 to April 23, 1986 for "Novel Si-Based Materials and Device Structures by Molecular Beam Epitaxy". Research findings in four scientific areas, (a) MBE growth, (b) heterojunction properties, (c) superlattice and quantum well structural devices, and Si on insulator by MBE are summarized. Details of these results are referred to the journal publications attached. In addition to scientific publications, the results of this research also help industrial development of commercial molecular beam epitaxy systems in U.S.

2. INTRODUCTION

Molecular beam epitaxy (MBE) has become a versatile technique for growing epitaxial semiconductor alloys and metal films in fabrication of a variety of structures.[1-3] Using MBE many unique features can be incorporated in the epitaxial growth. First, MBE growth temperatures can be from 450 to 650 C and are much lower than that required for liquid phase epitaxy (LPE) or chemical vapor deposition (CVD). This greatly reduces thermal stress due to the difference in thermal expansion that is set up on cooling and can thus reduce resultant dislocations at the interface. Diffusion of dopants in the materials or interdiffusion at the interface is reduced by using growth temperatures. Second, providing an atomically clean surface of silicon for growth under ultra-high vacuum conditions offers the best control of interface impurities. Finally, MBE techniques offer the ultimate in thickness control of very thin layers as needed for high frequency devices. With these unique attributes, a number of novel semiconductor multi-layer structures with dimensions comparable to those of lattice spacing or even atomic dimension in the direction of growth have been produced by MBE.[4-6] Most of the previous MBE efforts have been, however, in the investigation of growth, properties and the application of III-V compound semiconductors, focusing mainly on GaAs and $Al_xGa_{1-x}As$.[1-3] Devices, such as enhanced mobility FETS,[7-8] modulation doped devices,[9-10] which are capable of operating with an extremely high speed, have been made. Using the conduction band discontinuity of heterojunctions, electrons can be confined in a potential well as a two-dimensional gas. Impurity atoms have been deposited some 5 to 10 nm away from a narrow channel for the confined electron gas. In this case an enhanced electron

mobility as high as 1 x 10^6 $cm^2v^{-1}s^{-1}$ AT 4.2^oK has been observed, due to Debye screening of the impurity Coulombic scattering.

In this report, we describe the progress and the scientific findings made upon completion of the contract performed for "Novel Si-based Materials Device Structures by Molecular Beam Epitaxy". We have executed most of proposed tasks. In some cases, new directions were taken. For example, in the area of finding new approaches of growing Si on insulator, we have used Si on porous Si approach in lieu of the originally proposed lateral growth method. The result of taking the new direction enables us to obtain large sizes of SOI structures of greater 350 μm.

The progress made in the contractual period is summarized below. Detailed descriptions are referred to the papers published as attached in the appendices.

In the following sections, we will first describe the recent progress of Si MBE and its current status along with the successful growth of strained layer lattices using Ge_xSi_{1-x}/Si and silicide/Si. Then unexplored properties of superlattices and hetero quantum well structures by Si MBE will be discussed, to be followed by a description of potential devices based upon several different classes of Si-based superlattices.

(a) MBE growth

High quality Si MBE films can be grown if suitable initial preparation is stipulated to provide a clean surface at the beginning, and an adequate steady-state ultra high vacuum and clean environment are maintained throughout the growth.

Usually, a Si surface may be cleaned by heating the substrate to a temperature beyond 1200°C to remove the common contaminants, O and C [11]. However, for MBE to be a viable technology, exposure of the sample to such

an excessive high temperature must be circumvented; otherwise the most important and unique low temperature attribute of Si MBE is lost. Recent research results have shown that a repetitive oxidation of the surface in boiling HNO_3 and removal of the oxide in HF in cleaning wafers is an effective means of removing all C and heavy metal contaminants; at the final step, a thin oxide is subsequently grown in the mixture of H_2O_2 and HF (or other mixtures) prior to loading the sample into the UHV [12]. This thin oxide is used to protect the surface against added C contamination on the Si surface during the subsequent handling in sample loading. The thin oxide is then decomposed in-situ in the growth chamber just prior to growth at about 850°C [13]. Fig. 1 shows an Auger electron signal of the C and O as the substrate is flashed. The open data are for the conventional cleaning and the solid data for the new technique. Experiments have also demonstrated that a low flux Si beam incident on the thin protective SiO_2 film during the flashing can effectively reduce the decomposition temperature to below 750°C [14]. Another technique of surface cleaning is to ion-sputter the Si surface with low energy Ar^+ (<1000 eV) to remove a layer of the surface along with all impurity atoms, followed by a few minutes of annealing at 850°C [15]. The annealing releases the Ar atoms from Si and repair the damage caused by the ionic impact. This technique appears quite effective in removing the common contaminants; devices and superlattices have been grown. However, re-contamination from the ambient may occur during the in-situ annealing and the question remains as to how completely the damage is repaired by this short low temperature annealing and how sensitive electrical properties such as the resulting carrier lifetime and pn junction leakage are affected. The low temperature decomposition (cleaning) procedure nicely complements the use of ion

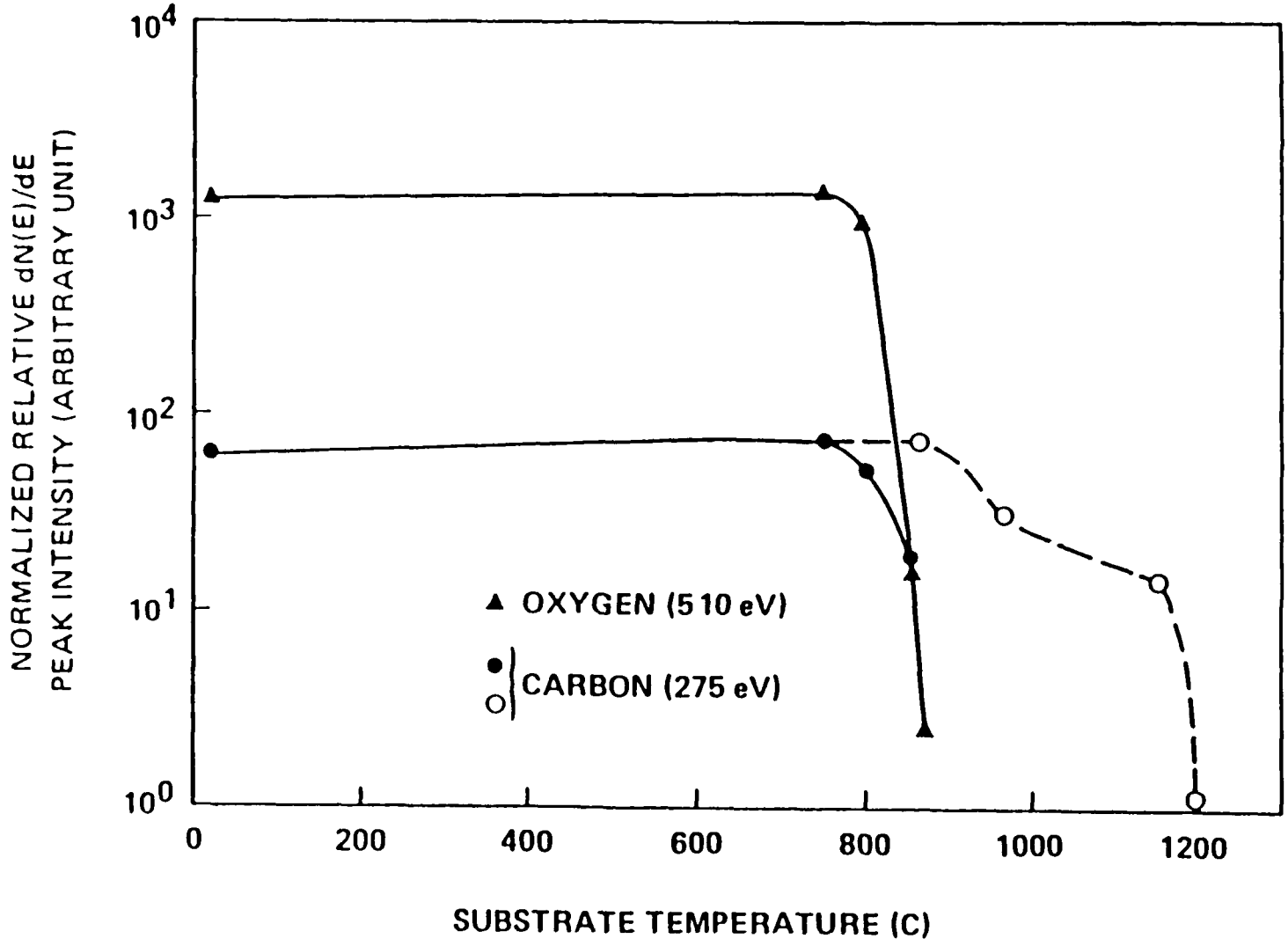


Fig.1 AES signal intensity as the substrate being flash-heated at different temperatures. The open data are for the conventional cleaning technique while the solid data are for the new cleaning method.

sputtering cleaning and the two make repetitive growth of superlattices and other heterojunction possible.

Another area of progress is in doping control. In Si MBE, Sb and Ga are usually thermally-evaporated as n- and p-type dopants, respectively. However, they are found to exhibit low incorporation ratios, i.e., low ratios of the dopant concentration in the grown film to the corresponding surface adlayer. In spite of the complex incorporation behavior, Iyer, Metzger and Allen [16] have successfully achieved sharp doping profiles by applying flash-off and pre-buildup techniques to adjust the surface adlayer concentration. However such techniques require interruption of the epitaxial process, which causes added contaminants to be introduced and further, the control of adlayers become cumbersome for superlattice and multilayer growth [13]. In addition, the maximum doping density afforded by these thermal dopants is usually low and the applications for fabrication of many types of devices are severely limited [12,15].

Recent progress has shown capabilities of providing high densities and abrupt doping profiles. Among these is the use of ion doping by secondary implantation [17]. Secondary implantation differs from direct low energy ion implantation in that the Si ions (e.g., originating from the e-gun heated source) interact with the dopant adlayer and causes the incorporation ratio to increase, rather than directly ion implanting the dopant ions into Si [17]. Previously, low energy direct ion implantation has been used but residual damage was evident if the annealing (or growth) temperature is kept low (i.e., below 800°C) [18]. Another approach is using electron bombardment (1.4 KeV) of the Si surface to affect the incorporation ratio [19]. By applying these techniques, abrupt doping profiles for n-type (Sb doping) with a doping density up to 3×10^{19} cm^{-3}

have been obtained. For p-type doping, thermal boron (B) sources, which can provide a high incorporation ratio, have been used to replace Ga. Ga in contrast with B has another disadvantage of having a high acceptor ionization energy, 70 meV. This high ionized energy limits the saturation carrier concentration to below 2 x $10^{18}/cm^3$ if Ga is used. However, pure atomic B sources are difficult to use owing to the refractory nature of B (low vapor pressure) and other impurities (and thus contamination) often accompany B evaporation. A recent work reports the use of an alternative source material, B_2O_3 [20]. The high vapor pressure of B_2O_3 permits a low operation temperature of the source in providing B doping. We have demonstrated that when evaporating B_2O_3 arrives at the surface, it decomposes and oxygen escapes from the surface; B is incorporated into the film. These major advances suggest that the doping in Si MBE may soon be brought into control.

(b) Heterojunction properties and devices

More significant is the successful growth of several heterostructures $CoSi_2$/Si (or $NiSi_2$/Si) [21-23]. For example, our group has investigated the growth kinetics of $CoSi_2$ under various conditions and the result shows that high crystalline and morphologically uniform $CoSi_2$ films can be grown using MBE with a proper flux stoichiometry and temperature control. Fig. 2a shows channelling and random RBS spectra of a $CoSi_2$ MBE film, illustrating a near perfect crystalline film. The uniform surface morphology of the MBE film is obtained by scanning electron microscopy as shown in Fig. 2b, in contrast with pinholes (and island growth) present using solid phase epitaxial reaction. Si/$CoSi_2$/Si and Si/$NiSi_2$/Si heterostructures have also been fabricated. These heterojunctions offer possibility to improve many conventional devices as well as for exploring

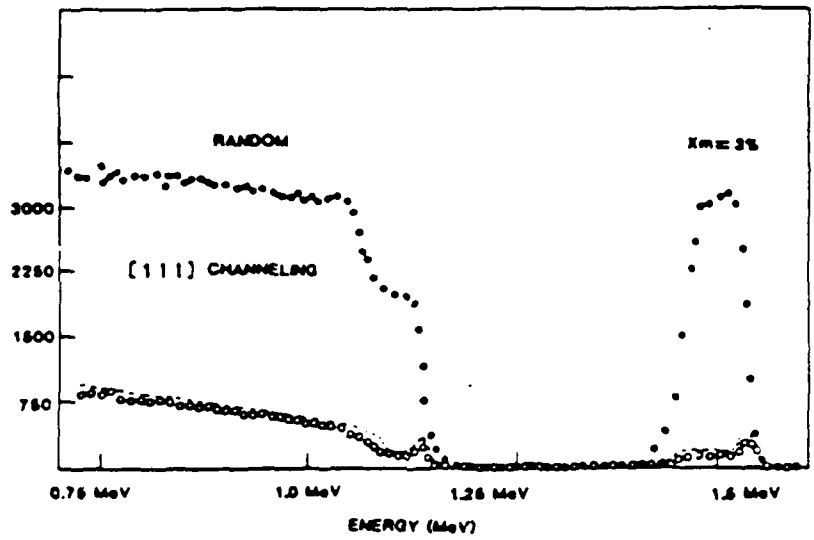
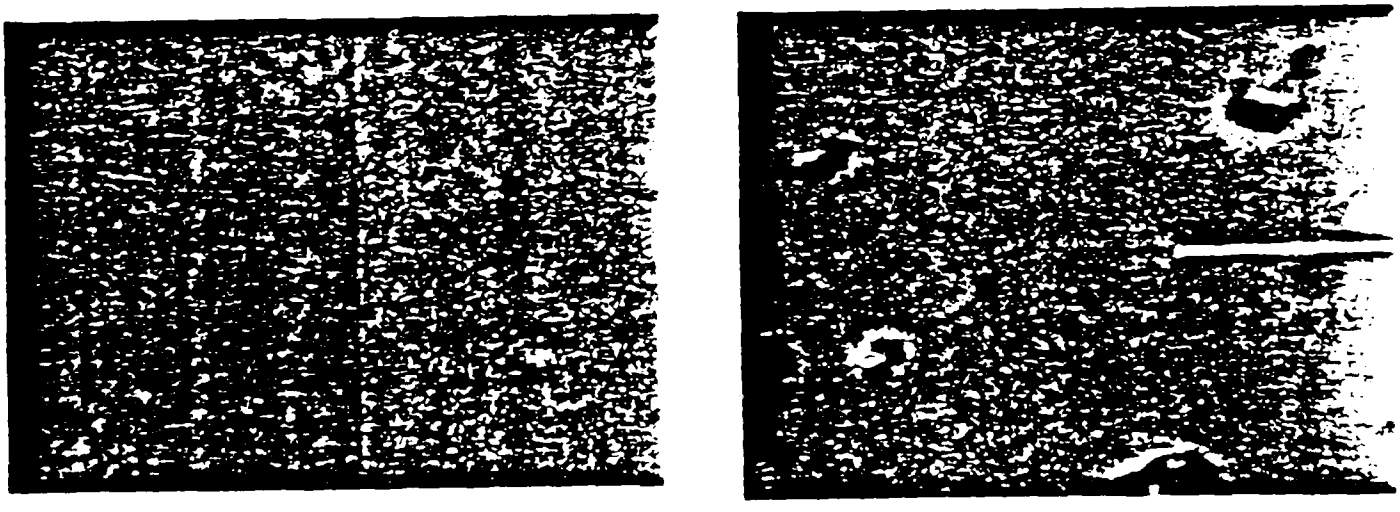


Fig. 2a Random and channeling RBS data of MBE $CoSi_2$.



MBE SPE film

Fig. 2b SEM micrography showing a morphologically smooth $CoSi_2$ grown by MBE, in contrast with the presence of pinholes in SPE film.

new ones. For example, a metal base transistor, which uses a thin silicide as the base, can achieve high speed performance without the constraints of conventional bipolars, although the gain is usually low due to the base scattering and the quantum mechanical reflection at the collector interface [24]. Indeed, recent results show the usually predicted low current gain [21,25]. In addition, pinhole conduction due to growth problems appears to be present in some cases. The pinhole problem has been in part resolved using MBE with a controlled flux ratio by this investigator's group.

Si Permeable Base Transistors (PBT) [26] using a Ni_2Si_2 and $CoSi_2$ grid buried epitaxially as illustrated in Fig. 3 shows good promise [25]. In this case, the use of epitaxial metallic silicide circumvents the problem of the growth of the semiconductor overlayer occurring in nonepitaxial cases, such as that of tungsten on GaAs. The work on Si permeable base transistors are being continued at UCLA as well as in other research groups.

The low value of current gain in metal base transistors (discussed previously) and other types of hot electron transistors may be improved by circumventing electron transport in the metal [24]. Applying PBT technology to bipolars as shown in Fig. 3, the base resistance of the conventional bipolar is reduced by using the epitaxial grid, which may be fabricated very much like PBT technology, known as a gridded bipolar transistor [27]. A wide gap emitter, Si in the case of the Ge_xSi_{1-x}/Si system, may be used to construct a heterogridded bipolar [28]. These devices may be fabricated using the MBE heteroepitaxial structures and there is an on-going effort at UCLA.

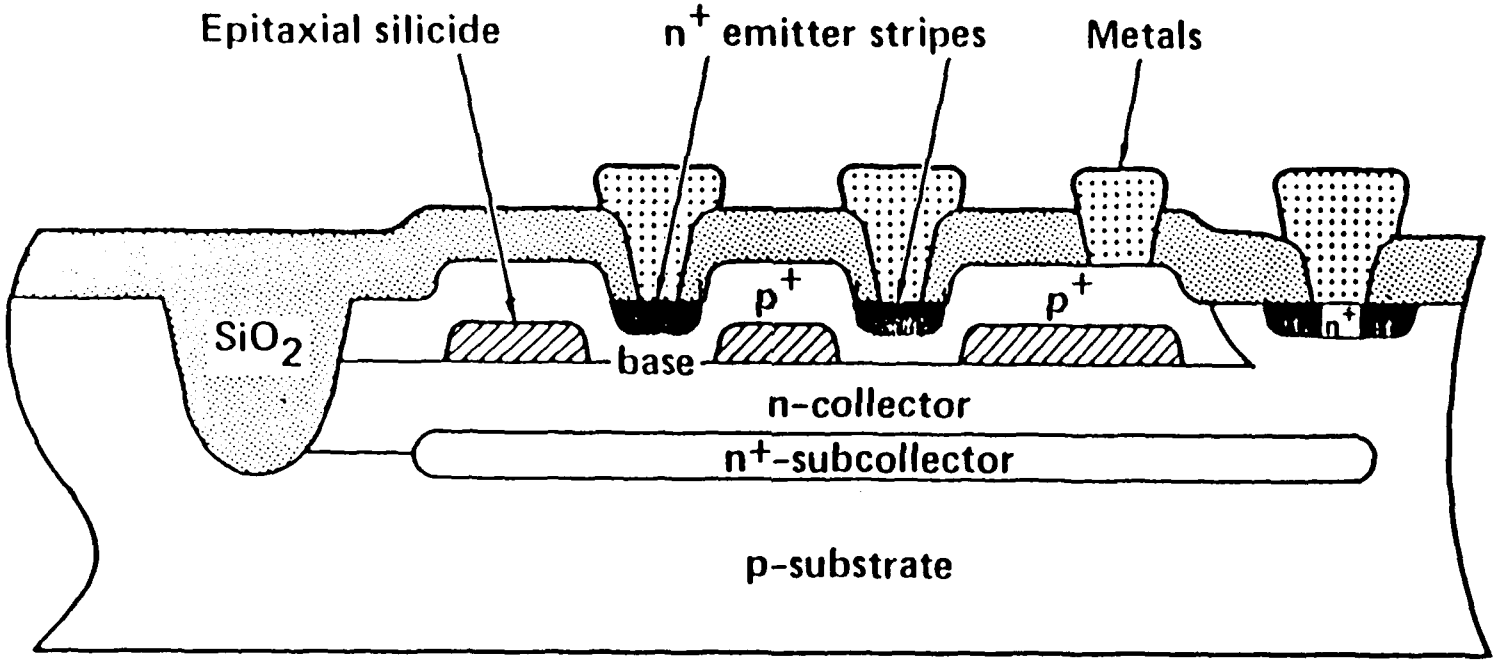


Fig. 3 Using buried epitaxial silicide ($CoSi_2$ or $NiSi_2$) as a grid in a bipolar transistor. The n^+ buried subcollector can be further replaced by the epitaxial silicide.

(c) Superlattice and multiple quantum well structure devices

Most appealing yet for Si MBE is to go beyond the simple heterojunction to building Si-based multiple quantum well (MQW) and superlattice devices. Several types of superlattices that can be grown with Si-based materials have been conceived. First, the alloyed superlattices using Ge_xSi_{1-x}/Si whose engineering of the bandgap is similar to that of the more familiar Al_xGa_{1-x} As/GaAs superlattice system may be used. The second type may consist of Si/silicide (particularly, $NiSi_2$ or $CoSi_2$) layers. The latter kind of superlattice has a unique and yet unexplored feature of having metallic layers in addition to semiconductor layers. The third type is the modulation-doped type of superlattices such as nipi structures. In this case, the doping density is varied to yield periodic or controllable quantum wells.

Similarly, we have begun the preparation for study of other Si based strained-layer superlattices, such as $Ge_{1-x}Si$/Si commensurate growth that has been recently demonstrated by Bean and coworkers and others. We are currently investigating the luminescence properties which have not been investigated extensively. Several interesting optical properties have been explored, leading to new directions of research which was submitted to the Army Research Office for funding. The preliminary growth of such superlattices is illustrated in an Auger analysis of the film shown in Fig. 4.

This research group at UCLA has recently succeeded in the growth of commensurate and morphological uniform $CoSi_2$ by MBE. Fig. 5 shows RBS channelling spectra for Si/$CoSi_2$/Si and Si/$CoSi_2$/Si/$CoSi_2$. In this case, the fine feature in the RBS spectra demonstrates crystalline layers. Unfortunately, the resolution is limited by the RBS technique in this case.

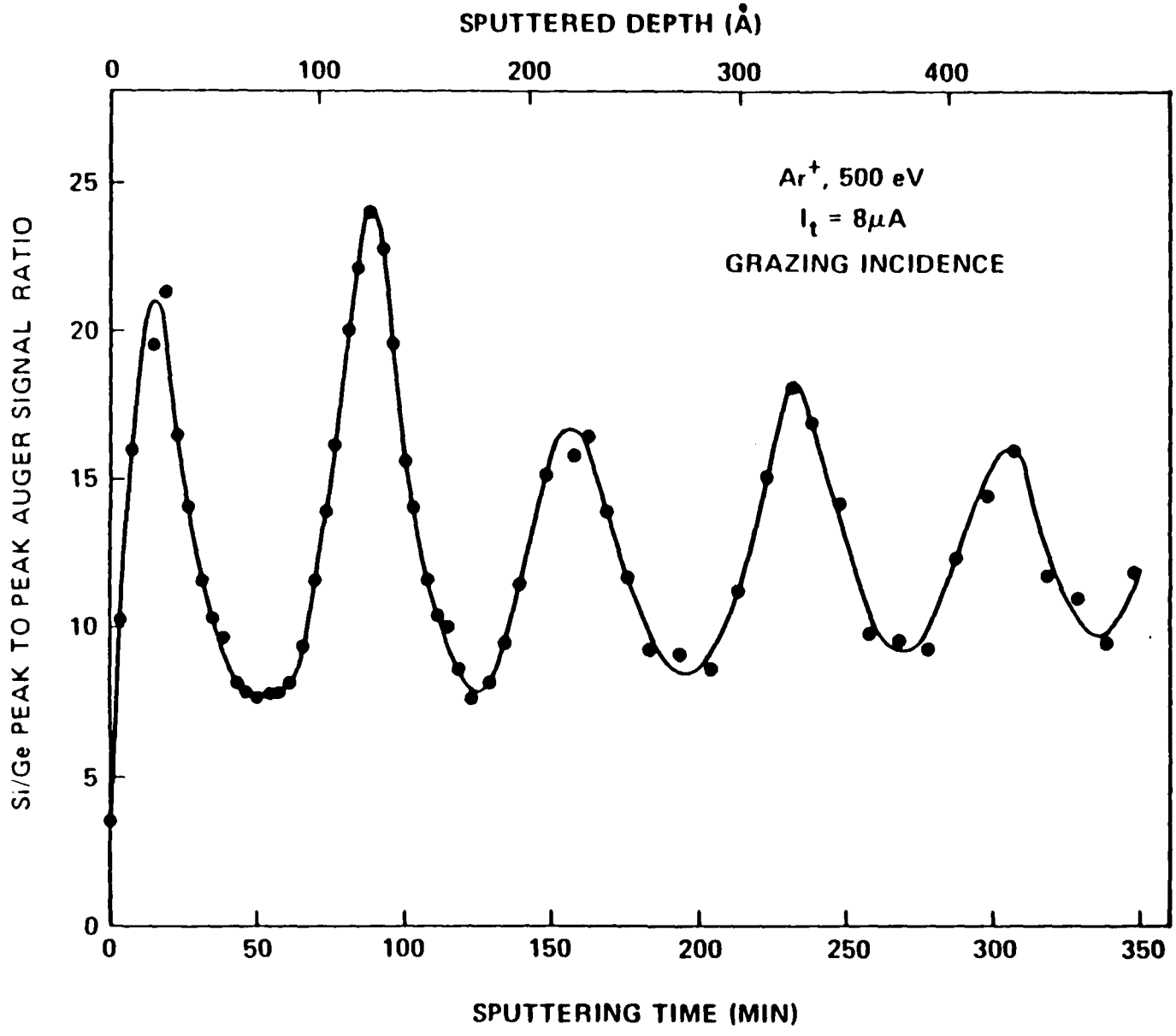


Fig. 4 Auger compositional depth profile of a Ge_xSi_{1-x}/Si superlattice.

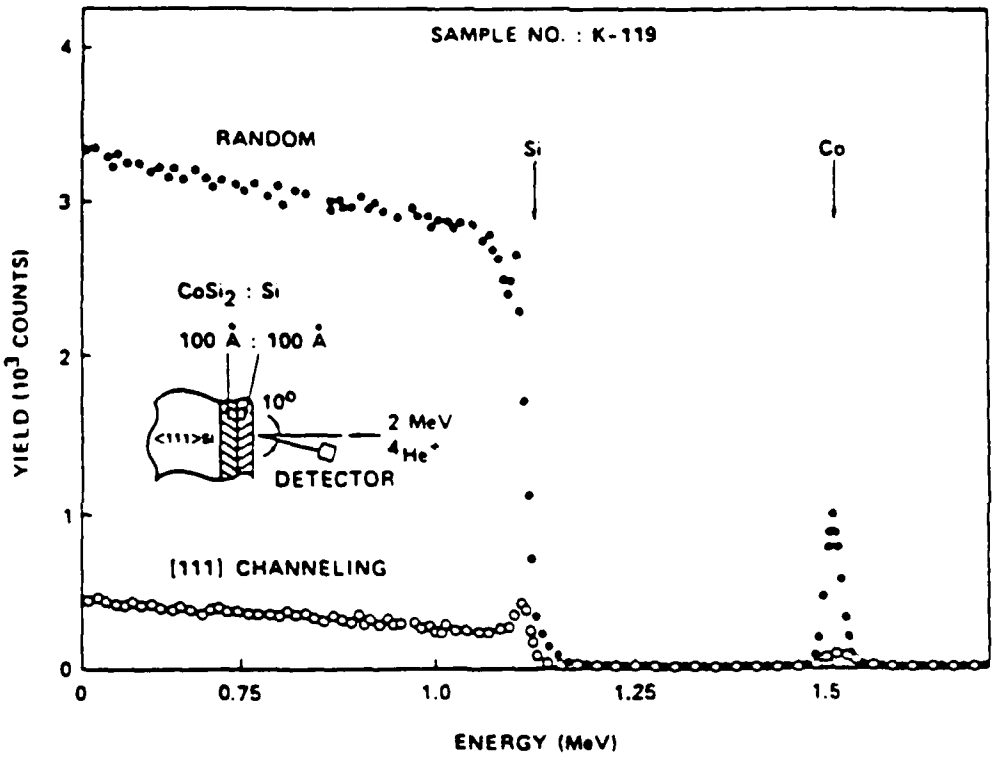
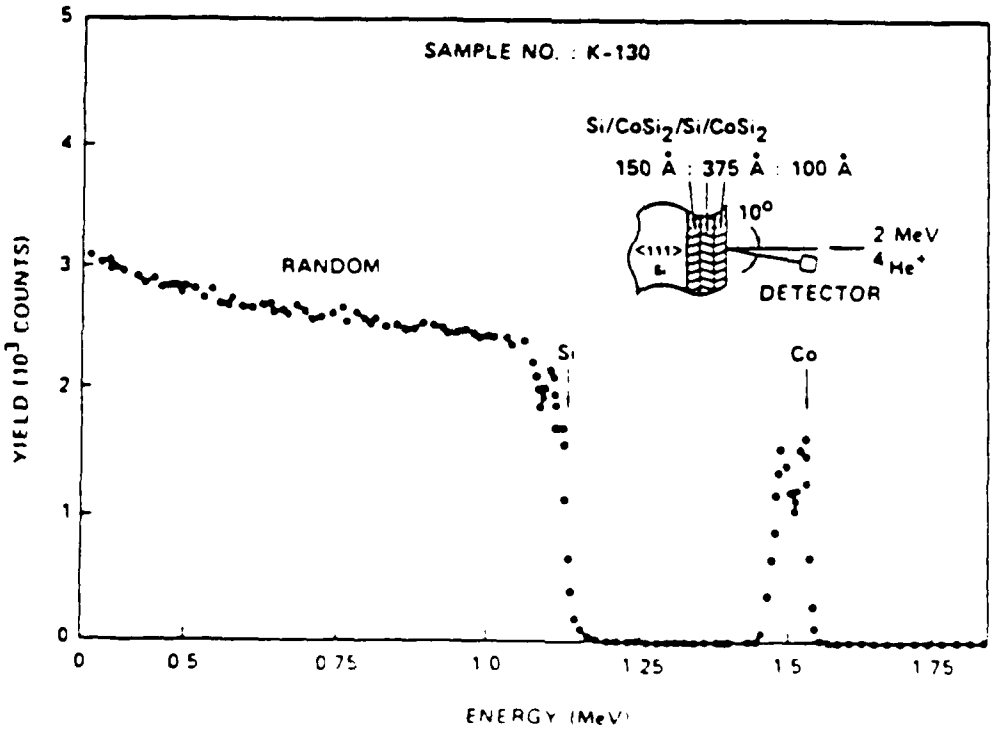


Fig. 5 RBS spectra for (a) $Si/CoSi_2/Si$ and



(b) $Si/CoSi_2/Si/CoSi_2$

There is a need for a better or higher resolution technique for the characterization of superlattices. Nevertheless, this success is the first demonstration of the epitaxial metal/semiconductor superlattices.

Many interesting and unique quantum mechanical phenomena need to be explored with these superlattices. For example, the confined two-dimensional electron gas and one-dimensional quantization can result high speed devices and extremely sensitive photo detectors. For example, Fig. 6 illustrates a tunnelling superlattice device that is conceived recently from these types of Si-based superlattices [29-30]. The optical properties in this type of structures is extremely important to explore. Although growth of the alloy superlattices have been preliminarily done as discussed previously, a more extensive study on growth is needed to improve and control the epitaxial quality for superlattices and multiple quantum well structures.

(d) Silicon on Insulator by MBE

Silicon-on-insulator (SOI) is very attractive for VLSI application because of its potential for high speed and high package density. It has been reported that porous silicon prepared from a crystalline substrate retains its crystallinity so that an epitaxial layer can be grown onto it.[31] However, if porous silicon was exposed to temperatures above 800^{o}C, such as during the conventional CVD epitaxial growth, the structure of pores collapses and the oxidation rate is dramatically reduced.[32] Since silicon molecular beam epitaxy (Si-MBE) can grow epi-film at temperatures as low as 600^{o}C,[33] the technique is ideal for preparing epi-films while maintaining the porosity of the porous silicon. By using Si-MBE growth on porous silicon and subsequently oxidizing the porous silicon through lithographically patterned Si windows, porous silicon can be

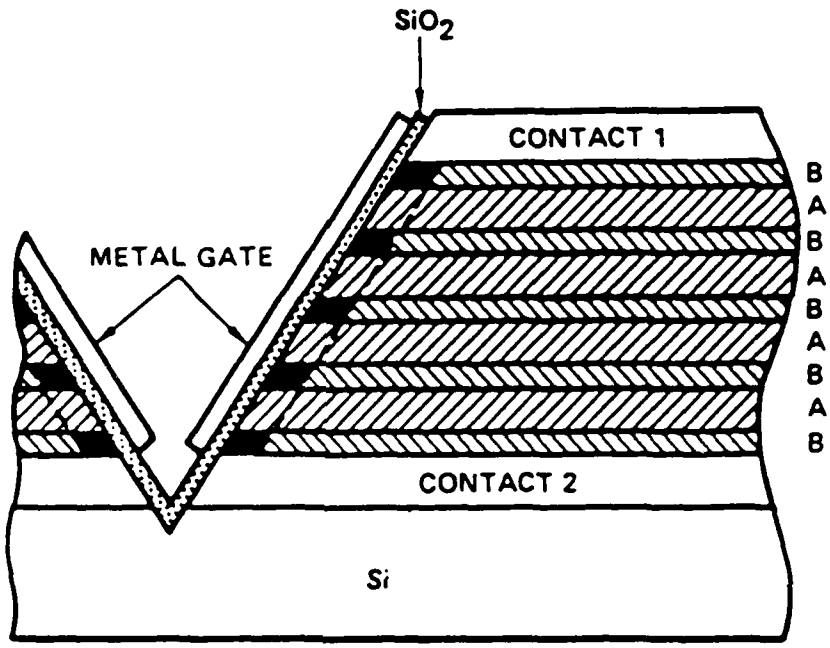


Fig. 6 A quantum well structure. A's are, for example, Si barrier layers while B's are Ge_xSi_{1-x} well layers. The tunneling current may be controlled by changing the barrier height with gate bias.

oxidized rapidly and laterally underneath the Si-MBE film due to the high oxidation rate of porous silicon; a SOI structure is accomplished.[34] in this contract period, we have demonstrated the use of a low temperature silicon beam surface cleaning method for porous silicon sample prior to the Si-MBE growth, and a two-step Si-MBE growth technique in achieving 100 micron wide SOI islands.

In experiments, porous silicon was fabricated by anodizing p^+ single-crystal wafers in a hydrofluoric acid electrolyte. A revised method using a low flux Si beam was used to in-situ clean the porous silicon surface prior to MBE. It has been reported that below a critical flux, the Si beam reacts with SiO_2 to form SiO which evaporates in the UHV chamber at a temperature as low as 700°C due to its high vapor pressure.[35] By carefully adjusting the Si beam flux, surface cleaning is accomplished for subsequent MBE growth. In the Si beam surface cleaning process, a Si beam with a flux of $7E13cm^{-2}sec^{-1}$ is used and the porous silicon sample is held at 750°C. The effectiveness of this method is checked by Auger Electron Spectroscopy (AES) and the etch pit density of as-grown MBE films after being Schimmel-etched. Fig. 6 shows the AES peak-to-peak amplitude ratios of both oxygen and carbon to silicon as a function of cleaning time. The oxygen peak is markedly reduced but remains at a small value (the reason discussed in the published paper) .

Si-MBE layers are then grown on porous silicon at 750°C immediately following the surface cleaning to avoid any re-comtamination by the residual gases in the UHV chamber. A two-step growth technique is used; the first layer of 500 Å thick is grown at a lower rate ($0.2Åsec^{-1}$) followed by a second layer of the desired thickness at a higher growth rate ($2Åsec^{-1}$). The first layer is used to buffer out the roughness of porous

silicon surface. Fig. 7 shows the minimum channeling yield of the RBS channeling spectra as a function of Si-MBE film thickness. The inset illustrates the RBS channeling spectrum for a sample having a 0.42 micron Si-MBE film grown on the porous silicon; a minimum yield X_m of 3% is identical to that of single-crystal silicon. The minimum channeling yield is greatly improved after a Si-MBE layer was grown on the porous silicon compared to the virgin porous silicon which has a minimum yield of 22.4%. The film crystallinity improves further as the Si-MBE film thickens; as the thickness of the Si-MBE film exceeds 0.24 micron, the minimum yield obtained is close to that of ideal single-crystal Si. The electron mobility of the Si-MBE film is measured by the van der Pauw method. An electron mobility as high as 1300 $cm^2V^{-1}sec^{-1}$ was obtained for an antimony-doped Si-MBE film having a doping concentration of $6x10^{15}cm^{-3}$.

The SOI structure is fabricated by wet-oxidized at 750°C after Si-MBE growth to grow a 500Å buffer SiO_2 layer. Then, a 2000Å thick Si_3N_4 was deposited on the SiO_2 layer by low pressure chemical vapor deposition (LPCVD). After lithographical patterning, Si islands were formed by removing Si_3N_4, SiO_2 and the Si-MBE film using plasma etching, buffered hydrofluoric acid and reactive ion etching, respectively. Then the samples were wet oxidized at 900°C for 4 hours. During the oxidation, the porous silicon was oxidized through the window openings and the oxidation fronts moved laterally and rapidly underneath the Si-MBE film until they met. Then, the Si-MBE islands were completely isolated by SiO_2 and the SOI structures accomplished.

In conclusion, a silicon beam method was successfully used as a low temperature surface cleaning method for porous silicon prior to Si-MBE growth.

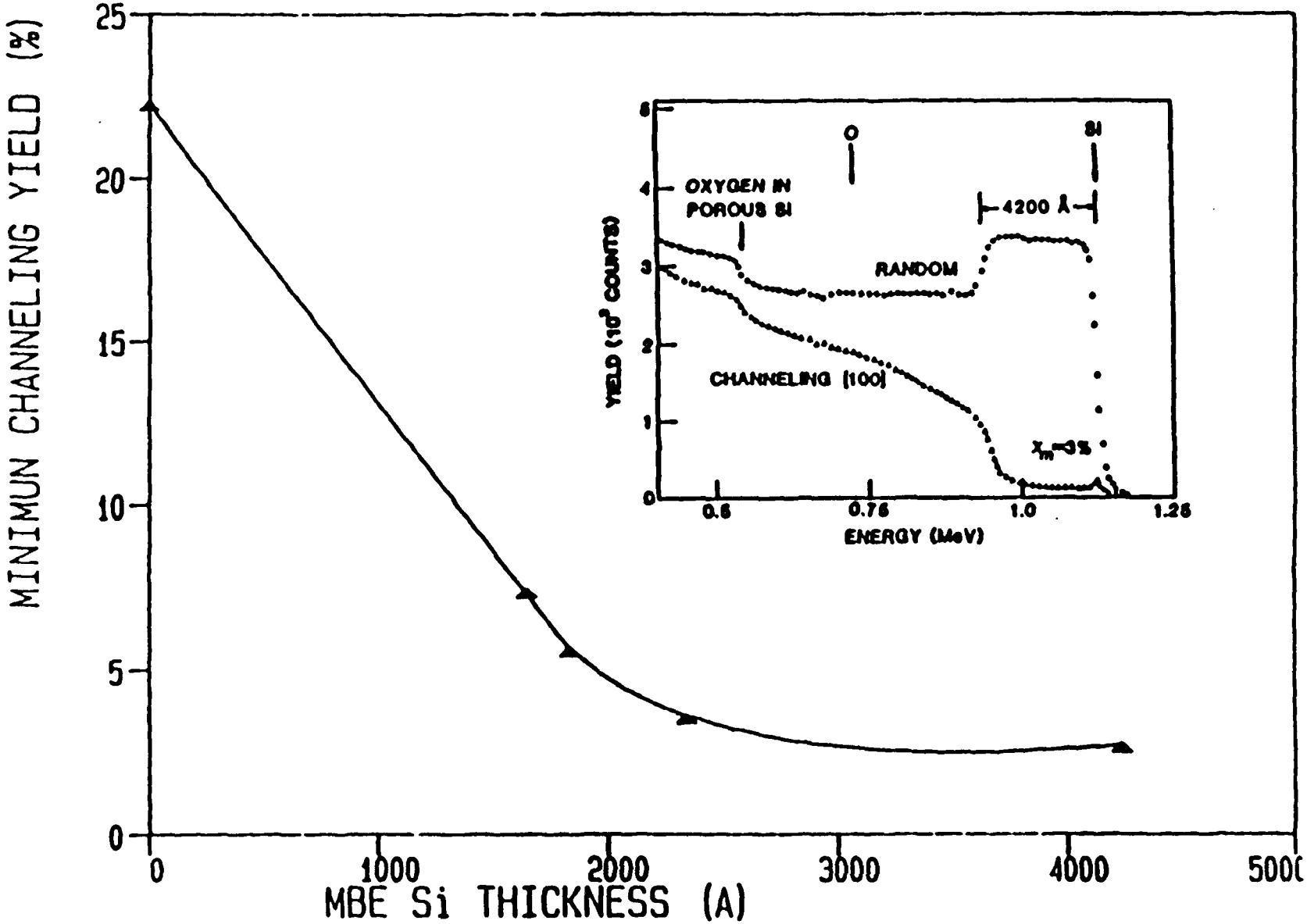


Fig. 7 RBS minimum channeling yield for various Si-MBE film thicknesses. Inset is the RBS of a sample with 4200 Å thick Si-MBE film on porous silicon. Oxygen is observed in the porous silicon region.

RBS shows that the tail of the AES oxygen signal is due to residual oxygen sitting on the pore walls which can not be reached by Si beam, and consequently should not have any effect on the following Si-MBE growth. The etch pit density of the as-grown Si-MBE film is below 1.7E3cm^{-2}. The RBS channeling spectrum of the Si-MBE film on porous silicon has a minimum yield of 3% showing a good crystallinity. The crystallinity of the Si-MBE film on porous silicon samples improves as the Si-MBE film thickens. An electron mobility of 1300 $cm^2V^{-1}sec^{-1}$ was measured by the van der Pauw method for an antimony doping concentration of 6E15cm^{-3}. SOI islands as large as 350 micron wide are successfully fabricated.

4. INDUSTRIAL IMPACT

During this research period, we have received recognization of our research effort. As a result, commercial MBE manufactures have requested our assistance in developing MBE. We are currently working jointly with the Perkin Elmer MBE Division to develop the first of the US Si MBE products. The impact and the contribution to the future Si technology can be very significant.

5. PUBLICATIONS AND GRADUATE STUDENTS TRAINING

4.1 Publications supported by this contract fund.

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Contributions to Seminars and Conferences:

Wang, K. L., "High-Speed Device Research in Silicon and Silicide MBE", IBM Thomas J. Watson Research Center, Yorktown heights, New York, Nov. 16, 1983. (Invited Talk)

Wang, K. L. "High Speed Devices and Transport Studies," Gould Colloquium (invited talk), 17 Nov. 1983, Chicago.

Wang, K. L. Session Chairman, 3rd Int'l. Conf. on Molecular Beam Epitaxy, Aug. 1-3, 1984, San Francisco: "MBE Growth on Si and Metals"

Wang, K. L., Li, G. P., Jogai, B. "Power-Frequency Scaling of Multilayered Microwave Devices," Int'l Conf. on Superlattices, Microstructures, and Microdevices, Aug. 13-17, 1984, Champaign, III. (Invited paper).

Wang, K. L. "High-Speed and High-Frequency Structures Using Molecular Beam Epitaxy Si and Silicide," 1984 Int'l Electronic Devices and Materials Symposium, Sept. 4-6, 1984, Hsinchu, Taiwan. (Invited Paper).

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Nicolet, M-A., Kao, Y. C., Tejwani, M., Wang, K. L., Hamdi, A. H. "Strain Measurements in Epitaxially Grown $CoSi_2$," Materials Research Society Annual Meeting, Nov. 26-30, 1984, Boston. (Invited Paper).

Xie, Y. H., Wang, K. L., Kao, Y. C., "An Investigation on Surface Conditions for Si Molecular Beam Epitaxial (MBE) Growth," 31st American Vacuum Society National Vacuum Symposium, Dec. 4-7, 1984, Reno, NV. (Invited Paper).

Wang, K. L., "Silicon and Metal-Silicide Molecular Beam Epitaxy," Golden Gate Metals Conf., Feb. 12, 1985, San Francisco (Invited Talk).

Xie, Y. H. and Wang, K. L., "Control of Schottky Barrier Heights by Solid Phase Epitaxy in Ultra-High Vacuum", March Meeting of American Physical Society, Baltimore, 1985.

Jogai, B. and Wang, K. L., "Tunneling Current of Finite Superlattices with Various Well-Widths and Barrier Heights", March Meeting of the American Physical Society, Baltimore, 1985.

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Lin, T. L., Chen, S. C., Wang, K. L., Iyer, S., "Si-MBE SOI," Materials Research Society, Fall Meeting, Boston, December, 1985.

Wang, K. L., "Properties and Applications of Molecular Beam Epitaxial Silicides", SPIE's Optoelectronics and Laser Applications in Science and Engineering, Los Angeles, January, 1986. (Invited Paper).

Wang, K. L. "The Physics of SOI Processing", American Physical Society Meeting, Las Vegas, March 31 - April 4, (1986). (Invited talk).

Lin, T. L. and Wang, K. L. "Silicon-on-insulator (SOI) Structure by Silicon Molecular Beam Epitaxial (Si-MBE) Growth on Porous Silicon", American Physical Society Meeting, Las Vegas, March 31 - April 4, (1986).

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de Frésart, E., Xie, Y. H. Rhee, S. S. and Wang, K. L., "Interaction of B_2O_3 with Si Surface in silicon-MBE Growth", the 28th Annual Electronic Materials Conference of the AIME, Amherst, Massachusetts, June 25-27, (1986).

4.2 Graduate student training

The research contract funding has been supporting graduate students in their M.S. Thesis and Ph.D. Dissertation research. During this contractual period, four Ph.D. students have completed their studies. Currently, they are employed by IBM, AT&T Bell Laboratories, and Rockwell International.

S. C. Chen	M.S.
P. M. D. Chow	Ph.D.
R. Faez	Ph.D.
G. P. Li	Ph.D.
T. L. Lin	M.S.
Ya Hong Xie	Ph.D.
E. de Frésart	Postdoctoral
M. Tejwani	Postdoctoral

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